PATENT ABSTRACTS OF JAPAN

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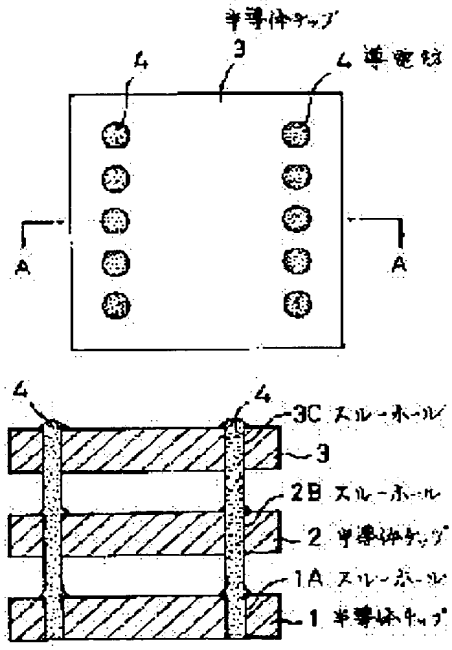
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To obtain a multilayer structure constructed of an increased number of layers and to realize an integrated circuit having high packaging efficiency by a method wherein a plurality of semiconductor chips each having a plurality of through holes are stacked with a prescribed gap between them and these chips are connected electrically by a conductive material through the through holes in a plurality.
CONSTITUTION: Semiconductor chips 1, 2 and 3 are stacked one by one with a prescribed gap between them and connected electrically by a conductive material 4 through through holes 1A, 2B and 3C provided in each chip. By providing the through holes 1A, 2B and 3C in a plurality in each of the semiconductor chips 1, 2 and 3 in a plurality and by connecting them electrically by the conductive material 4 through the through holes 1A, 2B and 3C thereof, in other words, a multilayer semiconductor device can be constructed of many layers stacked. The semiconductor device having packaging efficiency about ten times higher than the ones of usual examples can be manufactured and also a large effect to reduction of the cost is obtained.



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[Date of registration]
[Number of appeal against examiner's decision of rejection]

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[Date of extinction of right]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device which has a predetermined interval, carries out a laminating in the height direction, and is characterized by connecting the aforementioned semiconductor chip electrically by the electric conduction material which let the aforementioned through hole pass for two or more semiconductor chips which have two or more through holes.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the semiconductor device which can carry the high integrated circuit of packaging density.
[0002]
[Description of the Prior Art] In recent years, increase of the gate scale of a semiconductor integrated circuit is being enhanced, and it has also expanded the area of a semiconductor chip according to it. In the industrial world, the high semiconductor integrated circuit of packaging density has been developed with technology, such as multilayering of a package, to this problem. Also in it, technology which makes a surface mount a printed circuit board using a bump came to be performed in the industrial world in a semiconductor integrated circuit.
[0003] The plan and drawing 4 which show the composition of the semiconductor device of the former [drawing 3] are the B-B cross section of drawing 3 . For the semiconductor chip of an upper case, and 7, as for A pad of the semiconductor chip 6 of an upper case, and 9, in drawing 3 and drawing 4 , the semiconductor chip of the lower berth and 8 are [5 / a bump and 6 / B pad of the semiconductor chip 7 of the lower berth and 10] wire bonding pads.
[0004] Creation of the above-mentioned semiconductor device forms two or more bumps 5 who become the A pad 8 formed on the semiconductor chip 7 of the lower berth from a metal. And the B pad 9 corresponding to the A pad 8 is formed on the semiconductor chip 7 of the lower berth in which the surrounding wire bonding pad 10 was formed, and thermocompression bonding of the semiconductor chip 7 of the lower berth is carried out to these B pads 9 through a bump 5. By this composition, the semiconductor chips 6 and 7 of an upper case and the lower berth perform up-and-down composite-ization, and are aiming at improvement in mounting efficiency.
[0005]
[Problem(s) to be Solved by the Invention] However, with the above-mentioned conventional composition, since it was a laminating means by the bump, it had the fault that the multilayering more than two-layer was difficult in a semiconductor chip, and improvement in the mounting efficiency beyond this could not be aimed at.
[0006] this invention solves the above-mentioned conventional trouble, multilayers a large number more, and aims at offer of the high semiconductor device of a degree of integration.
[0007]
[Means for Solving the Problem] In order that this invention may attain the above-mentioned purpose, the laminating of two or more semiconductor chips which have two or more through holes is carried out in the height direction with a predetermined interval by the electric conduction material which let the aforementioned through hole pass, and it is characterized by connecting the aforementioned semiconductor chip electrically.
[0008]
[Function] According to this invention, through a through hole, the multilayering to the height direction of two or more semiconductor chips is possible, and a semiconductor device with more high mounting efficiency can be obtained by electric conduction material.
[0009]

[Example] The plan and drawing 2 which show the composition of a semiconductor device [in / one example of this invention / in drawing 1] are the A-A cross section of drawing 1 . In drawing 1 and drawing 2 , 1-3 are the electric conduction material which let a semiconductor chip, 1A2B, and 3C to the through hole of each semiconductor chips 1, 2, and 3, and let 4 pass to the aforementioned through hole.

[0010] The semiconductor device of this invention is the composition that let through hole 1A prepared in each semiconductor chip, 2B, and 3C pass when it had a predetermined interval in the height direction and each semiconductor chips 1, 2, and 3 were accumulated on it one after another, and each semiconductor chip was electrically connected by the electric conduction material 4.

[0011] Thus, according to this example, a semiconductor chip is accumulated in the height direction with a predetermined interval, and it is possible to multilayer to many layers by preparing a through hole in each, letting the through hole pass, and connecting electrically by electric conduction material.

[0012] In addition, although the semiconductor chip consists of three sheets as an example, you may make number of sheets increase further in this example.

[0013]

[Effect of the Invention] As explained above, by accumulating two or more semiconductor chips in the height direction with a predetermined interval, and connecting these by electric conduction material electrically, the semiconductor device of this invention can make the high semiconductor device of about 10 times [of the conventional example] mounting efficiency, and also brings a big effect to curtailment of cost.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the plan showing the composition of the semiconductor device in one example of this invention.
[Drawing 2] It is the A-A cross section of drawing 1 .
[Drawing 3] It is the plan showing the composition of the semiconductor device in the conventional example.
[Drawing 4] It is the B-B cross section of drawing 3 .
[Description of Notations]
1, 2, 3 -- Semiconductor chip 1A, 2B, 3C -- Through hole 4 -- Electric conduction material.

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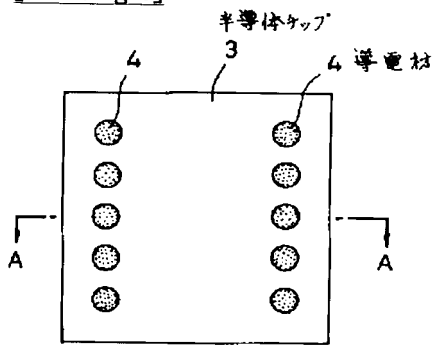
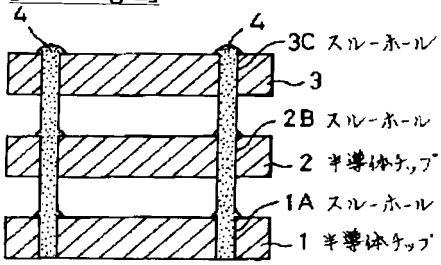
DRAWINGS

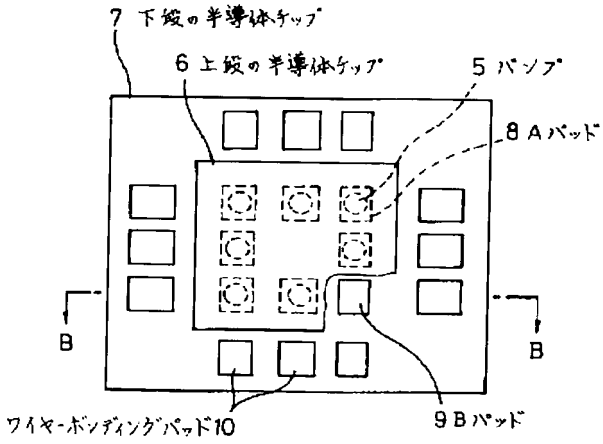
[Drawing 1]



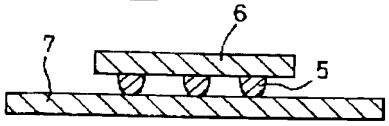
[Drawing 2]



[Drawing 3]



[Drawing 4]



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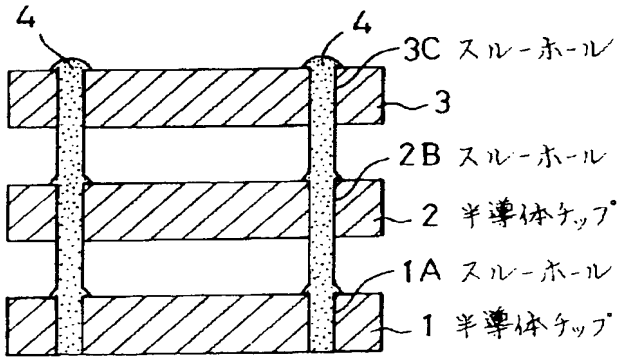
(54)【発明の名称】　半導体装置

(57)【要約】

【目的】　半導体チップを多層化することにより、実装効率の高い集積回路を実現する。

【構成】　複数の半導体チップ１，２，３を高さ方向に所定間隔をもって積み重ね、各半導体チップに設けられたスルーホール１Ａ，２Ｂ，３Ｃを通して、導電材４により電気的に接続する。



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【特許請求の範囲】

【請求項１】　複数のスルーホールを有する複数の半導体チップを、前記スルーホールを通した導電材により、高さ方向に所定の間隔をもって積層し、前記半導体チップを電気的に接続したことを特徴とする半導体装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、実装密度の高い集積回路を搭載することのできる半導体装置に関するものである。

【０００２】

【従来の技術】近年、半導体集積回路のゲート規模は増大の一途をたどっており、それに従って半導体チップの面積も拡大している。この問題に対して産業界では、パッケージの多層化等の技術をもって実装密度の高い半導体集積回路の開発を行なってきた。その中でも、半導体集積回路をバンプを用いてプリント基板に表面実装をする技術が産業界で行なわれるようになった。

【０００３】図３は従来の半導体装置の構成を示す平面図、図４は図３のＢ－Ｂ断面図である。図３および図４において、５はバンプ、６は上段の半導体チップ、７は下段の半導体チップ、８は上段の半導体チップ６のＡパッド、９は下段の半導体チップ７のＢパッド、10はワイヤーボンディングパッドである。

【０００４】上記半導体装置の作成は、下段の半導体チップ７上に形成された、Ａパッド８に金属からなる複数のバンプ５を設ける。そして、周辺のワイヤーボンディングパッド10が形成された下段の半導体チップ７上にＡパッド８に対応したＢパッド９を形成し、該Ｂパッド９と下段の半導体チップ７をバンプ５を介して熱圧着したものである。この構成により、上段，下段の半導体チップ６，７は、上下の複合化を行ない、実装効率の向上を図っている。

【０００５】

【発明が解決しようとする課題】しかしながら、上記従来の構成では、バンプによる積層手段となっているため半導体チップを２層以上の多層化は困難であり、これ以上の実装効率の向上を図ることはできないという欠点を有していた。

【０００６】本発明は、上記従来の問題点を解決するもので、より多数の多層化を行い、集積度の高い半導体装置の提供を目的とするものである。

【０００７】

【課題を解決するための手段】本発明は上記目的を達成するために、複数のスルーホールを有する複数の半導体

2

チップを、前記スルーホールを通した導電材により高さ方向に所定間隔をもって積層し、前記半導体チップを電気的に接続したことを特徴とする。

【０００８】

【作用】本発明によれば、スルーホールを通して導電材により複数の半導体チップの高さ方向への多層化が可能であり、より実装効率の高い半導体装置を得ることができる。

【０００９】

【実施例】図１は本発明の一実施例における半導体装置の構成を示す平面図，図２は図１のＡ－Ａ断面図である。図１および図２において、１～３は半導体チップ、１A２B，３Cは各半導体チップ１，２，３のスルーホール、４は前記スルーホールに通した導電材である。

【００１０】本発明の半導体装置は、各半導体チップ１，２，３を高さ方向に所定間隔をもって次々と積み重ねるとき各半導体チップに設けられたスルーホール１A，２B，３Cを通して、導電材４により各半導体チップが電気的に接続された構成である。

【００１１】このように本実施例によれば、半導体チップを所定間隔をもって高さ方向に積み重ね、そして、それぞれにスルーホールを設け、そのスルーホールを通して、導電材により電気的に接続することにより、何層にも多層化を行なうことが可能である。

【００１２】なお本実施例では、一例として半導体チップは３枚で構成されているが、さらに枚数を増加させてもよい。

【００１３】

【発明の効果】以上説明したように本発明の半導体装置は、複数の半導体チップを高さ方向に所定間隔をもって積み重ね、これらを電気的に導電材で接続することにより、従来例の10倍程度の実装効率の高い半導体装置を作ることができ、コストの削減にも大きな効果をもたらす。

【図面の簡単な説明】

【図１】本発明の一実施例における半導体装置の構成を示す平面図である。

【図２】図１のＡ－Ａ断面図である。

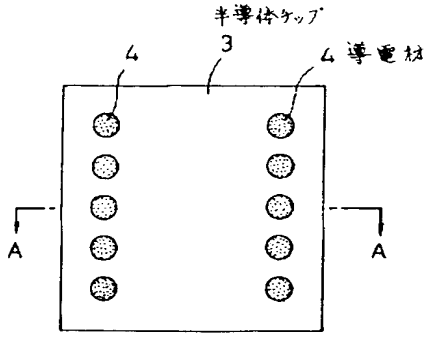
【図３】従来例における半導体装置の構成を示す平面図である。

【図４】図３のＢ－Ｂ断面図である。

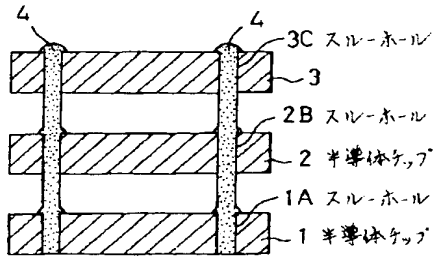
【符号の説明】

１，２，３…半導体チップ，　１A，２B，３C…スルーホール，　４…導電材。

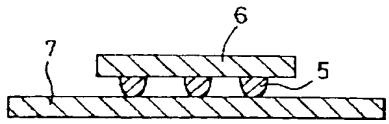
【図１】


半導体チップ
3
4
4 導電材
A
A

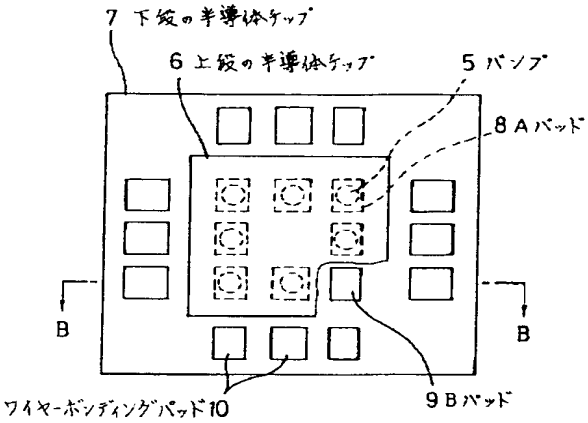
【図２】


4
4
3C スルーホール
3
2B スルーホール
2 半導体チップ
1A スルーホール
1 半導体チップ

【図４】


6
7
5

【図３】


7 下段の半導体チップ
6 上段の半導体チップ
5 バンプ
8 A パッド
B
B
ワイヤーボンディングパッド10
9 B パッド